Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A timing control method of a hardware-simulating program, a plurality of simulating elements being defined in said hardware-simulating program ~~and~~ to be executed in mixed sections as ~~in~~ a predetermined sequence, said timing control method comprising steps of:

a) referring to a time coordinate to realize a current time point when said hardware-simulating program has been executed to a certain degree; ~~and~~

b) suspending ~~and then restarting operations~~ execution of said predetermined sequence of said simulating elements if said current time point has not reached a specified time point yet, and continuing execution of said predetermined sequence of said simulating elements when said specified time point has been reached; and

c) repeating said steps a) and b) until said predetermined sequence is completely executed with different specified time points;

wherein an interval between a pair of said specified time points is independently adjustable so as to optionally change simulating speeds of said hardware-simulating program in different portions of said predetermined sequence.

2. (Currently Amended) The timing control method according to claim 1 further comprising steps of:

accumulating execution time of each of said simulating elements; and

determining said hardware-simulating program has been executed to said certain degree when said accumulated execution time of each of said simulating elements has reached or exceeded a threshold period;

wherein said threshold period is preset according to an operational speed of a simulated hardware.

3. (Cancelled).

4. (Currently Amended) The timing control method according to claim 2 wherein ~~a period from the simulation starting point to~~ said interval between said pair of specified time points is adjusted to be greater than ~~a multiple or reciprocal multiple of~~ said threshold period for decreasing the simulating speed in a portion of said predetermined sequence to be lower than the operational speed of the simulated hardware, or adjusted to be less than said threshold period for increasing the simulating speed in said portion of said predetermined sequence to be higher than the operational speed of the simulated hardware.

5. (Currently Amended) The timing control method according to claim [[4]] 2 wherein ~~said period from the simulation starting point to~~ said interval between said pair of specified time point is adjusted to be equal to said threshold period ~~so that~~ for approximating the simulation speed in a portion of said predetermined sequence to the operational speed ~~of said hardware-simulating program is equal to that~~ of the simulated hardware.

6. (Currently Amended) The timing control method according to claim 4 wherein said ~~period from the simulation starting point to said specified time point~~ interval is double of said threshold period so that the simulated speed executed by said hardware-simulating program in said portion of said predetermined sequence is a half of ~~that~~ the operational speed of the simulated hardware.

7. (Currently Amended) The timing control method according to claim 4 wherein said ~~period from the simulation starting point to said specified time point~~ interval is a half of said threshold period so that the simulated speed executed by said hardware-simulating program

in said portion of said predetermined sequence is double of ~~that~~ the operational speed of the simulated hardware.

8. (Currently Amended) The timing control method according to claim 2 wherein said hardware-simulating program is for simulating an instruction set executed when a microcontroller controls a plurality of peripheral devices, and said accumulated execution time of each of said simulating elements is accumulated by operating the count of executed machine commands with a machine cycle of said microcontroller.

9. (Cancelled)

10. (Original) The timing control method according to claim 1 wherein said time coordinate is a system clock.

11. (Original) The timing control method according to claim 1 further comprising steps of:

attaching time tags to simulation data associated with a specified simulating element;

storing said simulation data into a queue; and

reading out said simulation data from said queue according to said time tags when it is the turn of said specified simulating element to operate.

12. (Currently Amended) A timing control method of a hardware-simulating program, a plurality of simulating elements being defined in said hardware-simulating program ~~and~~ to be executed in mixed sections as ~~in~~ a predetermined sequence, said timing control method comprising steps of:

a) referring to a time coordinate to realize a current time point when accumulated execution time of each of said simulating elements is equal to or greater than a threshold; ~~and~~

b) performing a time-compensating operation if said current time point does not conform to an expected time point;

c) repeating said steps a) and b) until said predetermined sequence is completely executed with different expected time points;

wherein an interval between a pair of said expected time points is independently adjustable so as to optionally change simulating speeds of said hardware-simulating program in different portions of said predetermined sequence.

13. (Currently Amended) The timing control method according to claim 12 wherein when said current time point lags behind a corresponding one of said expected time points, said time-compensating operation is performed by suspending ~~the operations~~ execution of said simulating elements until said current time point advances to conform to said corresponding one of said expected time points.

14. (Currently Amended) The timing control method according to claim 12 wherein said interval between said pair of expected time points is equal to said threshold so that the simulation speed of said hardware-simulating program is equal to ~~that~~ an operational speed of ~~the~~ a simulated hardware.

15. (Currently Amended) The timing control method according to claim [[4]] 12 wherein said interval between said pair of expected time points is a multiple of said threshold so that the simulated speed by said hardware-simulating program is a reciprocal multiple of ~~that~~ an operational speed of ~~the~~ a simulated hardware.

16. (Currently Amended) The timing control method according to claim [[4]] 12 wherein said interval between said pair of expected time points is a reciprocal multiple of said threshold period so that the simulated speed by said hardware-simulating program is a multiple of ~~that~~

an operational speed of ~~the~~ a simulated hardware.

17. (Currently Amended) A recording medium recorded therein an accessible and executable hardware-simulating program, said hardware-simulating program defining therein a plurality of simulating elements, and said simulating elements being executed in mixed sections as ~~in~~ a predetermined sequence and automatically synchronized at intervals with a time coordinate of a system executing said hardware-simulating program, wherein said simulating elements are automatically synchronized by:

a) referring to said time coordinate to realize a current time point whenever said hardware-simulating program has been executed to a certain degree; ~~and~~

b) performing a time-compensating operation if said current time point does not conform to an expected time point;

c) repeating said steps a) and b) until said predetermined sequence is completely executed with different expected time points;

wherein an interval between a pair of said expected time points is independently adjustable so as to optionally change simulating speeds of said hardware-simulating program in different portions of said predetermined sequence.

18. (Currently Amended) A software platform for facilitating control program development, allowing a hardware-simulating program to work thereon, said hardware-simulating program defining therein a plurality of simulating elements, and said simulating elements being executed in mixed sections as ~~in~~ a predetermined sequence and automatically synchronized at intervals with a time coordinate of a system executing said hardware-simulating program, wherein said simulating elements are automatically synchronized by:

a) referring to said time coordinate to realize a current time point whenever said hardware-simulating program has been executed to a certain degree; ~~and~~

b) performing a time-compensating operation if said current time point does not conform to an expected time point;

c) repeating said steps a) and b) until said predetermined sequence is completely executed with different expected time points;

wherein an interval between a pair of said expected time points is independently adjustable so as to optionally change simulating speeds of said hardware-simulating program in different portions of said predetermined sequence.

19. (Currently Amended) The software platform according to claim 18 wherein said time coordinate is referred to realize a current time point when accumulated execution time of each of said simulating elements is equal to or greater than a threshold, ~~the operations~~ execution of said simulating elements are suspended when said current time point lags behind a corresponding one of said expected time points, and ~~the operations~~ execution of said simulating elements are restarted when said current time point advances to conform to said corresponding one of said expected time points.

20. (Currently Amended) The software platform according to claim 19 wherein said accumulated execution time of each of said simulating elements is calculated by timing the count of executed machine commands with a machine cycle of ~~the~~ a simulated hardware.